AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-16 (Canceled).

17. (Currently Amended) A processor clock control device operable to control switching between clock signals input to a processor, said processor clock control device comprising:

at least two clock signal inputs each operable to receive a clock signal, said clock signals comprising a first and a second clock signal;

a sensor operable to sense said first and said second clock signals;

a clock signal output operable to output a clock signal for input to a processor; and

a clock switching signal input for receiving a switching signal operable to control switching of said clock signal output from said first clock signal to said second clock signal; wherein:

said processor clock control device is operable on receipt of said switching signal to sense said first clock signal and if said first clock signal is at a second level when said switching signal is received, said processor clock control device is operable to hold said clock signal output at said second level, and then to sense said second clock signal and when said second clock signal transitions from ~~said~~ a first ~~predetermined~~ level to said second level to output said second clock signal.

18. (Previously presented) A processor clock control device according to claim 17, wherein following receipt of a clock switching signal, said clock switching signal input is inhibited from receiving further signals until said processor clock control device outputs said second clock signal.

19. (Previously presented) A processor clock control device according to claim 17, further comprising a plurality of set/reset flip flops and logic gates.

20. (Previously presented) A processor control device according to claim 17, further comprising a further clock signal input.

21. (Previously presented) A processing apparatus including the processor control device of claim 17.

22. (Previously presented) A processor clock control device operable to control switching between clock signals input to a processor, said processor clock control device comprising:

at least two clock signal inputs each operable to receive a clock signal, said clock signals comprising a first and a second clock signal;

a sensor operable to sense said first and said second clock signals;

a clock signal output operable to output a clock signal for input to a processor; and

a clock switching signal input for receiving a switching signal operable to control switching of said clock signal output from said first clock signal to said second clock signal, wherein:

said processor clock control device is operable on receipt of said switching signal to sense said first clock signal and when said first clock signal is detected at a second level, said processor clock control device is operable to hold said clock signal output at said second level, and then to sense said second clock signal and when said second clock signal transitions from said first predetermined level to said second level to output said second clock signal, and

said processor clock control device further comprises a further clock switching signal input operable to receive a further switching signal, said processor clock control device being operable to sense said second clock signal only after receipt of said further switching signal.

23. (Previously presented) A processor clock control device according to claim 22, wherein said processor clock control device is operable to sense said first clock signal and if said first clock signal is at said second level when said switching signal is received said processor clock control device is operable to hold said clock signal output at said second level.

24. (Previously presented) A processor clock control device according to claim 22, wherein said processor clock control device is operable to sense said first clock signal and when said first clock control device transitions from a first predetermined level to a second level said processor clock control device is operable to hold said clock signal output at said second level.

25. (Previously presented) A processor clock control device according to claim 22, wherein said further switching signal, comprises a switch signal component and a number component, said processor clock control device being operable to sense said second clock signal only after receipt of said switch signal component and to output said second clock signal for a number of cycles specified by said number component.

26. (Previously presented) A processor clock control device according to claim 22, wherein said clock switching signal input further comprises logic operable to inhibit forwarding of said received clock switching signal to said processor clock control device until said first clock signal reaches said first predetermined level.

27. (Previously presented) A processor clock control device according to claim 22, wherein said logic operable to inhibit forwarding of said received clock switching signal to said processor clock control device comprises a register that is clocked by said first clock signal at said first predetermined level.

28. (Currently Amended) A processing apparatus comprising:

a processor comprising a clock signal input;

at least two clocks each operable to output a clock signal; and

a processor clock control device according to claim ~~5~~ 26 being operable to control which one of said at least two clock signals is to be input to said processor clock signal input.

29. (Previously presented) A method of switching between clock signals to be output comprising the following steps:

outputting a first clock signal;

receiving a clock switching signal;

sensing a first clock signal and if said first clock signal is at a second level when the clock switching signal is received, holding said sensed first clock signal at said second level and outputting said held signal; and

sensing said second clock signal and when said second clock signal transitions from said first predetermined level to said second level, outputting said second clock signal.

30. (Previously presented) A method according to claim 29, comprising a further step:

following the step of receiving of said clock switching signal, inhibiting receipt of further input signals, and

following the step of outputting said second clock signal, allowing receipt of further input signals.

31. (Previously presented) A method of switching between clock signals to be output comprising the following steps:

outputting a first clock signal;

receiving a clock switching signal;

sensing a first clock signal and when said first clock signal is at a second level, holding said sensed first clock signal at said second level and outputting said held signal;

receiving a further switching signal, and after receipt of said further switching signal, sensing said second clock signal and when said second clock signal transitions from said first predetermined level to said second level, outputting said second clock signal.

32. (Previously presented) A method according to claim 31, wherein in said step of sensing a first clock signal, if said first clock signal is at said second level when said switching signal is received, holding said sensed first clock signal at said second level and outputting said held signal.

33. (Previously presented) A method according to claim 32, wherein in said step of sensing a first clock signal, if said first clock signal is at said first level when said switching signal is received sensing a transition from a first level to said second level and holding said sensed first clock signal at said second level and outputting said held signal.

34. (Previously presented) A method according to claim 32, wherein said further switching signal comprises a switch signal component and a number component, said step of sensing said second clock signal being performed only after receipt of said switch signal component and said step of outputting said second clock signal being performed for a number of cycles specified by said number component.

35. (Previously presented) A method according to claim 32, wherein said receipt of said clock switching signal is inhibited until said first clock signal reaches said first predetermined level.